REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02 tested at low dose rate. Make changes to paragraphs 1.2.2, 1.5, 4.4.1c, 4.4.4.1, Table I and figure 1. - ro	12-02-08	C. SAFFLE

REV																						
SHEET																						
REV	A	A	A	A																		
SHEET	15	16	17	18																		
REV STATUS			REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A				
OF SHEETS			SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

PREPARED BY
RICK OFFICER

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
RAJESH PITHADIA

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
10-12-16

AMSC N/A

REVISION LEVEL
A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, LINEAR, HIGH VOLTAGE, CURRENT SHUNT MONITOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-09244**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	R	09244	01	V	H	A
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

______________ ______________/
V
Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD8212	High voltage, current shunt monitor
02	AD8212	High voltage, current shunt monitor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
H	GDFP1-F10	10	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_S to COM)	68 V
V_{OUT} voltage	V_S to COM - 5.2 V
Reverse supply voltage (V_S to COM)	0.3 V
Power dissipation (P_D)	8 mW
Output short circuit duration	Indefinite
Maximum junction temperature (T_J)	150°C
Lead temperature (soldering, 10 seconds)	300°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	56°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	93°C/W 2/

1.4 Recommended operating conditions.

Supply voltage (V_S to COM)	7 V to 65 V 3/
Ambient operating temperature range (T_A)	-55°C to +125°C

1.4.1 Operating performance characteristics.

Input / output characteristics: (T_A = +25°C, +V_S to COM = 15 V)

Input impedance differential	2 kΩ
Input impedance common mode (+V_S to COM = 7 V to 65 V)	5 MΩ
Output impedance	20 MΩ
Input to output transconductance	1000 μA / V

Dynamic response: (T_A = +25°C, +V_S to COM = 15 V) 4/

Small signal bandwidth - 3dB (Gain = 10)	1000 kHz
Small signal bandwidth - 3dB (Gain= 20)	500 kHz
Small signal bandwidth - 3dB (Gain = 50)	100 kHz

Noise performance: (T_A = +25°C, +V_S to COM = 15 V)

Voltage noise (referred to input (RTI), f = 0.1 Hz to 10 Hz)	1.1 μVp-p
Voltage noise (referred to input (RTI), special density, f = 1 kHz)	40 nV / $\sqrt{Hz}$

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Measurement taken under worse case condition of still air.

3/ This device has high voltage operation which is achieved by using external voltage breakdown PNP transistor. In this configuration, the common mode range of the device is equal to the breakdown of the external PNP transistor. Refer to section 6.7 for more information.

4/ External input filtering should be considered to trade off desired dynamic response versus undesired response to system transients and electromagnetic interference (EMI). Refer to section 6.7 for more information.

1.5 Radiation features.

Device type 01:
Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) .... 100 krads(Si) 5/
Device type 02:
Maximum total dose available (dose rate ≤ 10 mrads(Si)/s) .... 50 krads(Si) 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

5/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

6/ For device type 02, radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition D.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 051 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_A \leq +125°C$ V_S to COM = 7 V to 65 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Total supply current 3/	I_S	$I_S = I_{OUT} + I_{BIAS}$, $7 V \leq +V_S \leq 65 V$, (normal operation)		1,2,3	01, 02		720	μA
			M,D,P,L,R	1	01		720	
			M,D,P,L	1	02		720	
		$I_S = I_{OUT} + I_{BIAS}$, 4/ high voltage operation, using external PNP transistor		1,2,3	01,02		1500	
			M,D,P,L,R	1	01		1500	
			M,D,P,L	1	02		1500	
Voltage offset section								
Offset voltage	V_{OS}	Gain = 1		1	01,02	-2	+2	mV
				2,3		-3	+3	
			M,D,P,L,R	1	01	-2	+2	
			M,D,P,L	1	02	-2	+2	
Offset voltage drift	$\Delta V_{OS} / \Delta T$	Gain = 1 5/		2,3	01,02	-10	+10	μV / °C
Input section								
Differential input voltage range	V_{IN}	Input voltage between $+V_S$ and V_{SENSE}		1,2,3	01,02	0	500	mV
			M,D,P,L,R	1	01	0	500	
			M,D,P,L	1	02	0	500	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input section								
V_{SENSE} input pin current	I_{SENSE}	$7\ V \leq +V_S \leq 65\ V$, (normal operation)		1,2,3	01,02		200	nA
			M,D,P,L,R	1	01		200	
			M,D,P,L	1	02		200	
		3/ 4/ 6/ High voltage operation, using external PNP transistor		1,2,3	01,02		1000	
			M,D,P,L,R	1	01		1000	
			M,D,P,L	1	02		1000	
Output section								
Output current range 3/	I_{OUT}	V_{IN} = 0 mV to 500 mV		1,2,3	01,02	0	500	μA
			M,D,P,L,R	1	01	0	500	
			M,D,P,L	1	02	0	500	
Circuit gain	G	$R_{shunt} = R_L = 1\ k\Omega$, 7/ V_{IN} = 50 mV and 500 mV		1,2,3	01,02	0.99	1.01	V / V
			M,D,P,L,R	1	01	0.99	1.01	
			M,D,P,L	1	02	0.99	1.01	
$+V_S$ to COM regulator section								
Regulator voltage	V_{REG}			1,2,3	01,02	4.80	5.20	V
			M,D,P,L,R	1	01	4.80	5.20	
			M,D,P,L	1	02	4.80	5.20	
Regulator power supply rejection ratio	PSRR	$\Delta V_{REG} / \Delta +V_S$		1,2,3	01,02	-100	100	μV/V
			M,D,P,L,R	1	01	-100	100	
			M,D,P,L	1	02	-100	100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_A \leq +125°C$ V_S to COM = 7 V to 65 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
$+V_S$ to COM regulator section - continued.								
Bias current 3/	I_{BIAS}	$7\ V \leq +V_S \leq 65\ V$ (normal operation)		1,2,3	01,02		220	µA
			M,D,P,L,R	1	01		220	
			M,D,P,L	1	02		220	
		High voltage operation 4/ 6/ using external PNP transistor		1,2,3	01,02	200	1000	
			M,D,P,L,R	1	01	200	1000	
			M,D,P,L	1	02	200	1000	
Minimum ALPHA pin input current	I_{ALPHA}	8/		1,2,3	01,02	25		µA
			M,D,P,L,R	1	01	25		
			M,D,P,L	1	02	25		
Rising step response settling time	t_{S_rise}	V_S = 0 - 15 V, 5/ 9/ R_{Shunt} = 1 kΩ, G = 20, V_{IN} = 0 m V - 500 mV, SR = 23 V/µs, V_{OUT} settling to 1%, see 4.4.1c		9,10,11	01,02		2.2	µs
Falling step response settling time	t_{S_fall}	V_S = 15 - 0 V, 5/ 9/ R_{Shunt} = 1 kΩ, G = 20, V_{IN} = 500 mV - 0 mV, SR = 23 V/µs, V_{OUT} settling to 1%, see 4.4.1c		9,10,11	01,02		1.5	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Device type 01 supplied to this drawing has been characterized through all levels M, D, P, L, and R of irradiation. Device type 02 supplied to this drawing has been characterized through all levels M, D, P, L of irradiation. However, device type 01 is only tested at the "R" level and device type 02 is only tested at the "L" level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A for device type 01 and condition D for device type 02. Device type 02 has been tested at low dose rate.

3/ The device supply current in normal voltage operation ($+V_S$ = 7 V to 65 V) is the bias current (I_{BIAS}) added to output current (I_{OUT}). Output current varies upon input differential voltage and can range from 0 µA to 500 µA. For high voltage operation mode with an external PNP transistor, refer to section 6.7 for more information.

4/ Maximum $+V_S$ voltage to COM dependent in the collector emitter voltage breakdown of the transistor. R_{BIAS} must be selected to ensure I_{BIAS} within specification via $I_{BIAS} = (+V_S - V_{REGmax}) / R_{BIAS}$. Refer to section 6.7 for more information.

5/ Parameter not tested post irradiation.

6/ The current of the amplifier into V_{SENSE} pin increases when operating in high voltage external PNP transistor configuration mode. Refer to section 6.7 for more information.

7/ Gain measured by (V_{OUT} at 500 mV - V_{OUT} at 50 mV) / (V_{IN} at 500 mV - V_{IN} at 50 mV).

8/ The ALPHA pin current in the high voltage operation using external PNP mode equals the I_B base current of the external PNP transistor. The I_B maximum current must not exceed this minimum I_{ALPHA} specification.

9/ Subgroups 9, 10, and 11 are tested initially as part of device characterization, after subsequent wafer lots and as part of design and process changes.

Device types	01 and 02	
Case outline	H	
Terminal number	Terminal symbol	Description
1	$+V_S$	Supply voltage (inverting amplifier input).
2	COM	Regulator low side.
3	BIAS	Bias circuit low side.
4	NC	No connection.
5	NC	No connection.
6	NC	No connection.
7	I_{OUT}	Output current.
8	ALPHA	Current compensation circuit input.
9	NC	No connection.
10	V_{SENSE}	Noninverting amplifier input.

FIGURE 1. Terminal connections.

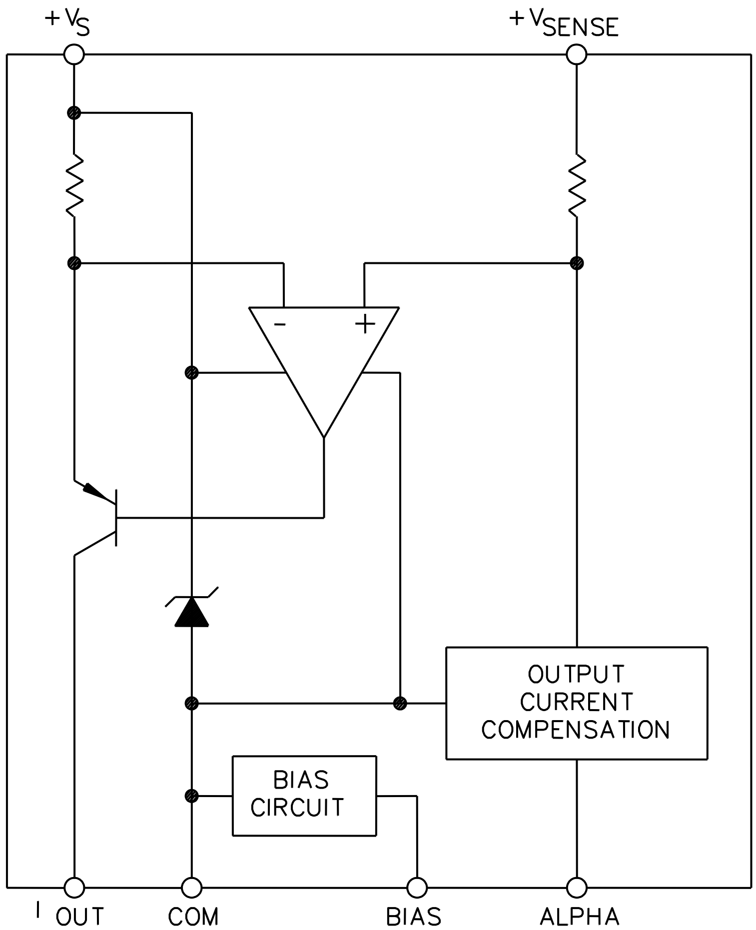

FIGURE 2. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 9, 10, and 11 are tested initially as part of device characterization, after subsequent wafer lots and as part of design and process changes.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 3/ 9,10,11	1, 2, 3, 1/ 3/ 9, 10, 11	1, 2, 3, 1/ 2/ 3/ 9,10,11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11 3/	1, 2, 3, 3/ 9, 10, 11	1, 2, 3, 3/ 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3 2/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table I).
3/ Subgroups 9, 10, and 11 are tested initially as part of device characterization, after subsequent wafer lots and as part of design and process changes.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/

Parameters	Symbol	Delta limits	Units
Bias current (normal operation)	I_{BIAS}	±10.00	μA
Offset voltage	V_{OS}	±0.40	mV
Gain	G	±0.0032	V/V

1/ If device is tested at or below delta limit in table, no deltas are required. Deltas are performed at room temperature.
2/ Delta parameters are performed at normal operation 7 V supply, normal operation 65 V supply, and with external PNP operation mode.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A for device type 01 and condition D for device type 02 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Application notes.

6.7.1 Normal operation (7 V to 65 V supply range). In normal applications as shown in figure 3, the device measures a small differential input voltage generated by a load current flowing through a shunt resistor. The operational amplifier (A1) is connected across the shunt resistor (R_{SHUNT}) with its inverting input connected to the battery/supply side, and the noninverting input connected to the load side of the system. Amplifier A1 is powered via an internal series regulator (depicted as a zener diode). This regulator maintains a constant 5 V between the battery/supply terminal of the device and COM, which represents the lowest common point of the internal circuitry. A load current flowing through the external shunt resistor produces a voltage at the input terminals of the device. Amplifier A1 responds by causing transistor Q1 to conduct the necessary current through resistor R1 to equalize the potential at both the inverting and noninverting inputs of amplifier A1.

6.7.1 Normal operation (7 V to 65 V supply range) - continued. The current through the emitter of transistor Q1 (I_{OUT}) is proportional to the input voltage (V_{SENSE}), and, therefore, the load current (I_{LOAD}) through the shunt resistor (R_{SHUNT}). The output current (I_{OUT}) is converted to a voltage by using an external resistor, the value of which is dependent on the input to output gain equation desired in the application.
The transfer function for the device is:

$I_{OUT} = (gm \times V_{SENSE})$ where: gm = 1000 µA / V.
$V_{SENSE} = I_{LOAD} \times R_{SHUNT}$,
$V_{OUT} = I_{OUT} \times R_{OUT}$,
$V_{OUT} = (V_{SENSE} \times R_{OUT}) / 1000$

When using the device as described, the battery / supply voltage (+V) in the system must be between 7 V to 65 V. The 7 V minimum supply range is necessary to turn on the internal regulator (shown as a zener). This regulated voltage then remains a constant 5 V, regardless of the supply voltage ($+V_S$). The 65 V maximum limit in this mode of operation is due to the breakdown voltage limitation of the device process. A 1% resistor can be used to convert the output current to a voltage where gain in V/V is set by R_{OUT} in kΩ.

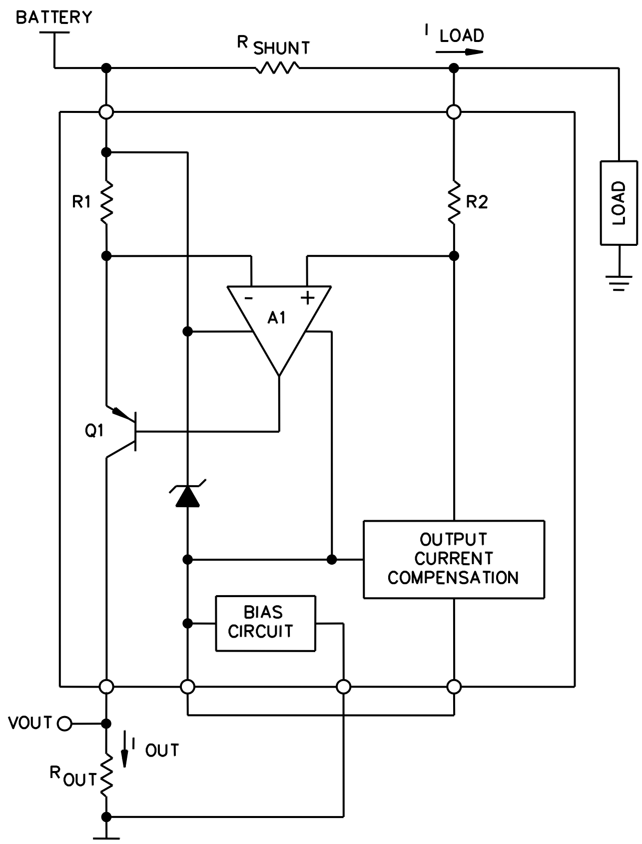

FIGURE 3. Normal configuration circuit.

6.7.2 High voltage operation using an external PNP transistor. In high voltage applications, the device can be configured as shown in figure 4. The device offers features that simplify measuring current in the presence of common-mode voltages greater than 65 V. This is achieved by connecting an external PNP transistor at the output of the device, as shown above. The VCE break-down voltage of this PNP becomes the operating common-mode range of the device. The device features an integrated 5 V series regulator. This regulator ensures that at all times COM, which is the most negative of all the terminals, is always 5 V less than the supply voltage (+V_S). Assuming a battery voltage (+V) of 100 V, it follows that the voltage at COM is (+V) – 5 V = 95 V. The base emitter junction of transistor Q2, in addition to the Vbe of one internal transistor, makes the collector of transistor Q1 approximately equal to 95 V + 2(Vbe(Q2)) = 95 V + 1.2 V = 96.2 V. This voltage appears across external transistor Q2. The voltage across transistor Q1 is 100 V – 96.2 V = 3.8 V. In this manner, transistor Q2 withstands 95.6 V and the internal transistor Q1 is only subjected to voltages well below its breakdown capability.

In this mode of operation, the supply current (I_{BIAS}) of the device circuit increases based on the supply range and the R_{BIAS} resistor chosen. For example if V+ = 500 V and R_{BIAS} = 500 kΩ, then, I_{BIAS} = (500 – 5) / 500 kΩ = 990 µA. In high voltage operation, it is recommended that I_{BIAS} remain within 200 µA to 1 mA. This ensures that the bias circuit is turned on, allowing the device to function as expected. At the same time, the current through the bias circuit / regulator is limited to 1 mA. Transistor Q2 can be a field effect transistor (FET) or a bipolar PNP transistor. The latter is much less expensive, however the magnitude of I_{OUT} conducted to the output resistor (R_{OUT}) is reduced by the amount of current lost through the base of the PNP. This leads to an error in the output voltage reading. The device includes a circuit at the ALPHA pin which compensates for the output current that is lost through the base of the external PNP transistor. This ensures that the correct transconductance gain of the amplifier is maintained.

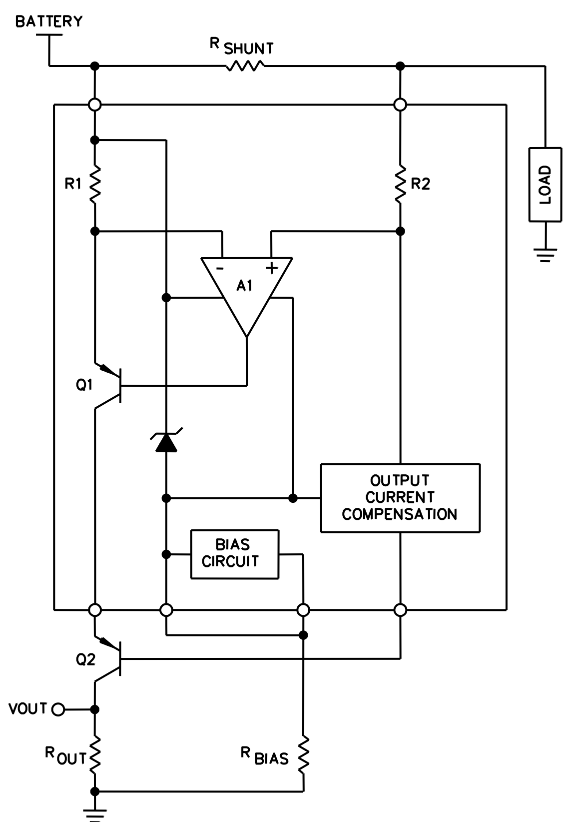

FIGURE 4. High voltage external PNP configuration circuit.

6.7.3 Dynamic response considerations. External input filtering should be considered to trade off desired dynamic response versus undesired responses to system transients and electromagnetic interference (EMI). External input filtering is achieved by adding the R_F / C_F filter circuit shown in figure 5. With the lower 2 kΩ input differential impedance, the R_F is recommended to be in the 5 Ω to 15 Ω range to prevent gain and CMR errors. With a R_F chosen, the C_F should be selected to achieve the desired low pass filter using the formula: Low pass filter cutoff frequency = 1 / (2 x π x R_F x C_F).

As an example, with R_F = 6 Ω and a C_F = 2.7 μF, the low pass filter (LPF) cutoff frequency will be 10 kHz. The chosen input filter cutoff frequency should suppress transients while allowing proper response to expected changes in the sensed current.

EMI suppression can also be achieved by using 1% tolerance capacitors on the $+V_S$ and $+V_{SENSE}$ inputs to ground. The capacitors must be matched and values selected based on suppression achieved with the 2 kΩ input differential impedance. Use the same low pass filter cutoff frequency equation replacing R_F with 2 kΩ. The chosen cutoff frequency should implement the EMI suppression while allowing proper response to expected changes in the sensed current.

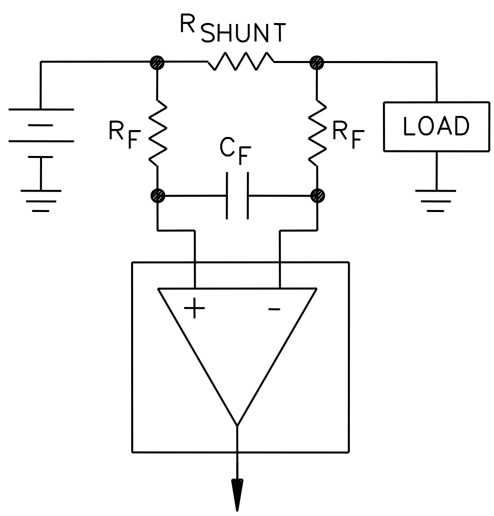

FIGURE 5. Input filter circuit.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-02-08

Approved sources of supply for SMD 5962-09244 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0924401VHA	24355	AD8212AL/QMLR
5962L0924402VHA	24355	AD8212AL/QMLL

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices (4) Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605